A New Simplified Spice Modelling of Memristor

Miljana Milić, Miljan Petrović

Abstract - In this paper we will introduce a new memristor model for Spice simulations that is computationally very inexpensive. It has four adjustable parameters, including low and high resistances and switching voltage threshold, and perfectly expresses memristive behaviour during simulations in transient domain. It is verified in LTspice simulations and shows good characteristics.

Keywords – Hysteresis, Memristor, Modelling, Simulation, Spice.

I. Introduction

Memristor as a component was first introduced by Leon Chua in 1971. as the fourth fundamental passive circuit element besides, resistors, capacitors and inductors [1]. It is characterized by the new physical parameter that is referred to as memristance, which creates dependence between the charge and the flux of the device. It took thirty-seven years after this prediction, for Hewlett Packard team lead by Stanley Williams to develop a first functioning solid-state memristor [2,3].

The relations between basic fundamental circuit elements and all electromagnetic quantities are shown in Fig.1.

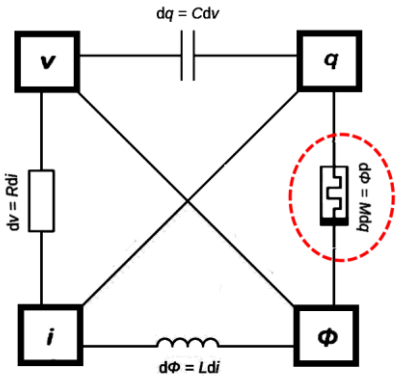

Fig. 1. Illustration of memristor as the missing circuit element

The research in the field of memristive devices has a significant importance due to a large potential of its applications in different areas of science: electronic, electrical, computational, bioengineering, neural etc.

Currently there are many unsolved questions related to the production of memristor, its modelling, simulating in a circuit and its applciations. All these problems depend on each other.

In this paper we will try to introduce a novel and a very simple Spice model of the memristor device, that can be used in a simulation of some simple circuit at first ie. for educational purposes. There are many models of memristor available in literature. There are few aspects of memristor modelling in which all these models compete: accuracy, complexity, possibilty to control threshold, possibility to be applied in different domains of circuit analysis, etc.

In order to develop a new model of the memristor and apply it into some novel application, it is necessary to have a good theoretical and applicative knowledge of the device. This will be done in the following section where we will give a brief overview of the memristor structure, physical, electrical and matematical behaviour, implementations, currently avaliable models and many different areas of applications. The third section describes a new Spice model of memristor. After that, we will verify the model in time domain simulations. The paper will be concluded with the ideas of its further development and applications.

II. Memristor Background

The first HP memristor was made of Titanium Dioxide creating two chemically different layers: one with high impedance and other that is conductive [4]. They were placed between two platinum electrodes. This is shown in Fig. 2. Titanium Dioxide normally behaves as an insulator, unless oxygen vacancies are introduced. Then it behaves as an n-type semiconductor. These oxygen vacancies affect the conductivity of the TiO_2, since they can drift when applied to varying electric field [5].

The mathematical model of HP memristor has two resistors connected in series, *Roff* and *Ron*, representing the undoped and doped fields of the component, respectively. It can be seen from Fig. 2 that the width of the memristor is denoted with *D*, while the width of the doped region is denoted with *w*. The width *w* represents a variable that changes with the charge [5].

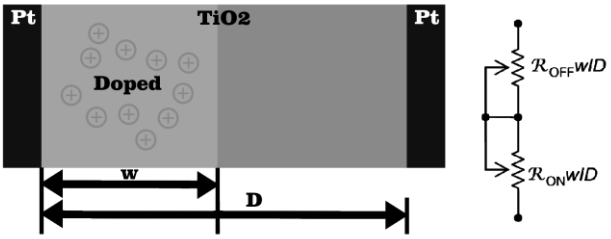

Fig. 2. HP memristor structure and its equivalent circuit

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The equivalent circuit for described structure is also shown in Fig. 2, while the corresponding *i-v* function for such a circuit is expressed with the two following equations:

$$v(t) = [R_{ON}\frac{w(t)}{D} + R_{OFF}(1-\frac{w(t)}{D})]\cdot i(t) \quad (1a)$$

$$\frac{dw}{dt} = \frac{\mu_v R_{ON}}{D} i(t) \quad (1b)$$

where μ_v denotes the mobility of ions [4, 5].

After the first Titanium Dioxide memristor, alternative materials were introduced for its implementation over last few decades. In 1963., a memristor made of ferroelectric material appeared [6]. In 2004. a polymeric (ionic) memristor was proposed [7]. A memristive behaviour occurred during the application of a resonant-tunnelling diode [8, 9]. Alternative memristor materials included also Graphene Oxide [10] and Silicon Oxide [11], while one of the alternative implementation is the spintronic memristive system described in [12].

Since its first appearance, many researchers were trying to demonstrate possible new applications of the new device [4]. All these applications can be categorized in a few groups. The first of them represents analogue circuits such as oscillators [13], programmable amplifiers [14], filters [15] and PLLs [16]. The second group is related to the neuromorphic circuits [17]. Chaotic systems are the fourth group of applications [18], whereas the last group incorporates the applications in digital circuits such as memories [19] and implementation of logic gates [20].

There are numerous models of memristor designed to emphasize different characteristics of the component. Some take into account the physical structure of the memristor [21, 22], and some exhibit only the memristor's functionality using generic Spice components [23, 24]. Although most of solutions are based on nonlinear modelling of memristor's characteristics [25, 26, 27], in this paper a linear model is proposed. Namely, memristor is modelled as a two-state resistor with ability of instant switching. This is useful for initial circuit simulation, especially for digital systems, such as memories.

III. SPICE MODEL

The memristor model described in this paper is a simplified model which provides a memristive behavior to circuit simulations. It does not take into account the physics and nanoelectronics of the real memristor component. Instead, it behaves as a two-state resistor and it is designed accordingly.

The schematic of the model is given in Fig. 3. As it can be seen, it consists primarily of behavioural voltage sources and some digital circuitry. Four parameters are defined as externals, meaning that their values are adjustable in the circuit which incorporates memristor component (they can vary from instance to instance). Those are *Ron*, low resistance of the memristor, *Roff*, high resistance of the memristor, *Vlim*, voltage threshold for switching between states, and *ton*, clock interval for the flip-flop which checks for the state of the memristor in the previous time instant.

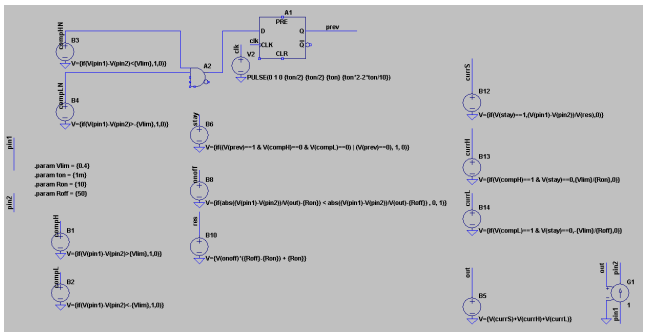

Fig. 3. Schematic of the described memristor model

Two nodes (*pin1* and *pin2*) represent external pins of the component. The memristor is modelled as voltage--controlled current source. However, all the behavioural sources in Fig. 3 are voltage sources, since Spice simulator does not allow nodes connected to current sources to "float". It is only after all the calculations, that the voltage-controlled current source (G1) with gain equal to 1 converts the output voltage into a current between nodes *pin1* and *pin2*.

Behavioural sources B3 and B4 function as comparators. They inspect whether the input voltage across the memristor is lower than the higher limit (*Vlim*), and higher than the lower limit (*–Vlim*, since the memristor *i-v* characteristic is modelled to be centrally symmetrical), and produce 1V output, accordingly. These two signals are passed through an AND circuit and fed into a D flip-flop controlled by an internal clock with period *ton*. On the other hand, behavioural sources B1 and B2 are comparators with slightly different functions, and they produce 1V if voltage across memristor is higher than *Vlim*, and lower than *–Vlim*, respectively, thus, denoting the current voltage across the memristor. Combining information from these comparators and "historical" information from the flip-flop, behavioural source B6 generates the voltage at a node *stay*, which is equal to 1V, only if it is not necessary (depending on the voltage conditions) to change the memristor's resistive state.

Further, the current resistance of the memristor is estimated with a behavioural source B8. It checks if the current resistance is closer to the value defined by *Ron*, or *Roff*, and sets the voltage at node *onoff* to 1V if the memristor is in the on state, and to 0V if the memristor is in the off state. The source B10 "translates" the information about the state (0 or 1 volts) to the voltage resistance. Namely, voltage at node *res*, is equal to *x* volts if the current resistance (*Ron* or *Roff*) equals *x* ohms.

Similarly, three voltage sources B12, B13, and B14 generate voltages at nodes *currS*, *currH*, and *currL*, respectively, and those are numerically equal to the appropriately generated currents. Source B12 gives the "current" equal to the ratio of voltage across the memristor and current resistance *res*, only if the component keeps its state. Sources B13, and B14 produce "current" if the state should be switched from high to low resistance (B13) or vice versa (B14). The "currents" are then limited as if they are produced by voltages *Vlim*, and *–Vlim*, in order to avoid extremely low or high values of current and voltage at switching time instances in simulation.

Finally, these "currents", modelled as voltages, are summed in the behavioural source B5, and, as it was aforementioned, converted into a current using component G1. Behaviour of the model in time domain is analysed in the following section of this paper.

III. SIMULATION

The memristor component is modeled in Spice as described in the previous section of this paper. Now, the model should be verified with a simple testbench. The circuit is fed with several different voltage waveforms, and the obtained behavior of the memristor is then analyzed.

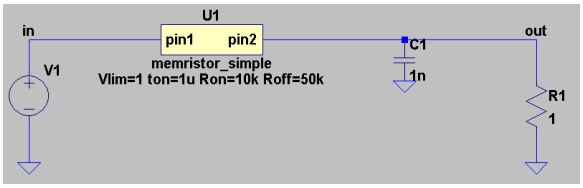

Fig. 4. Schematic of the testbench for memristor model simulations

The schematic of the testbench is shown in Fig. 4. It incorporates a voltage source V1 at the circuit input, a resistive load (1 Ω) at the output, while the main component i.e. the memristor is instantiated as the subcircuit U1. It is necessary to include a capacitor C1 (its initial value is 1nF) in order to slow down the ideal, instantaneous switching, controlled by behavioural sources inside the memristor, since that switching can lead to infinitesimal time step of the transient simulation, and further to a simulation crash. Values of memristor parameters are chosen as follows: voltage threshold is 1V, on and off resistances are 10kΩ and 50kΩ, respectively, and clock period is 1μs.

The first examined response of memristor is the response to the triangular input voltage. Since memristor's switch voltage was set to 1V, the amplitude of the input voltage is set to 1.005V. Four periods of the signals are plotted in Fig. 5. Voltage across the memristor is plotted with black line, and current through memristor with grey line. It can be seen that the slope of the current waveform alternates between lower and higher one. This is due to the switching of resistance that happens at each moment when the voltage signal reaches above 1V or below –1V, except at the first peak of 1.005V. The first voltage peak does not switch the memristor's state because the model still does not "know" what its previous state was. With the next ramp the memristor starts functioning. Further, resistance of memristor during this transient analysis is shown in Fig 5. It is obvious that the periods where resistance is either 10kΩ or 50kΩ correspond to the piece-wise linear parts of the triangular voltage signal.

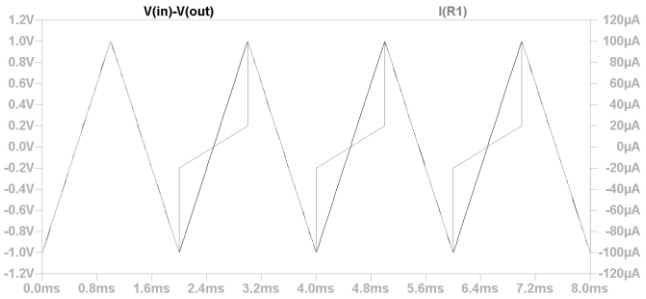

Fig. 5. Voltage across memristor and current through it for triangular voltage excitation

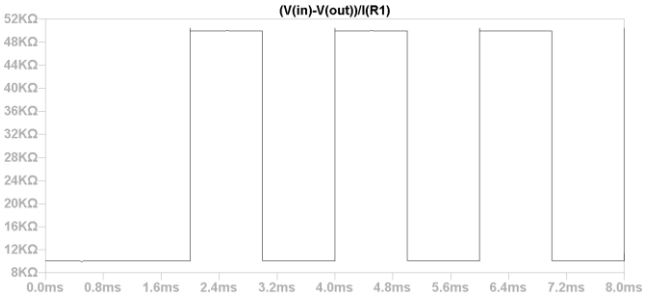

Fig. 6. Resistance of memristor for triangular voltage excitation

In order to get the current-voltage (*i-v*) characteristic of the memristor, one cannot use DC sweep, because of the presence of digital circuitry that memorize the previous state of the device model. Hence, this can be done only in transient analysis. Triangular input voltage signal is the appropriate one for it. Thus, we get the *i-v* characteristic as in Fig. 7. The well-known hysteresis of memristor can be recognized. Switching pieces of characteristic are close to ideal in the sense of infinite derivative (vertical lines in Fig. 7).

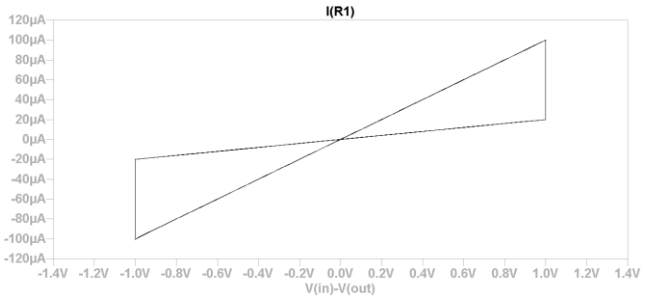

Fig. 7. I-V characteristic of memristor model

Sine and pulse voltage excitation are also applied in the testbench. Input voltage and output current of memristor for the sine wave input can be seen in Fig. 8. Input voltage and output current of memristor for the pulse wave input can be seen in Fig. 9. Amplitude of sine voltage is 1.005V, and the pulse wave switches between 1.005V and −1.005V.

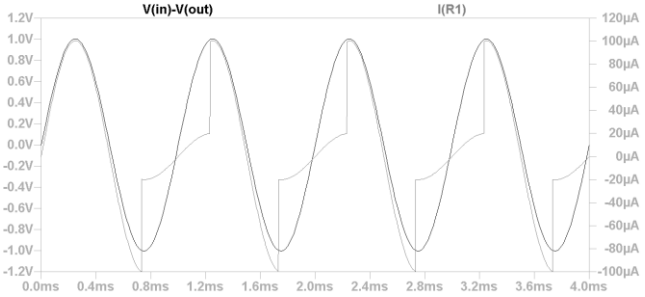

Fig. 7. Voltage across memristor and current through it for sine voltage excitation

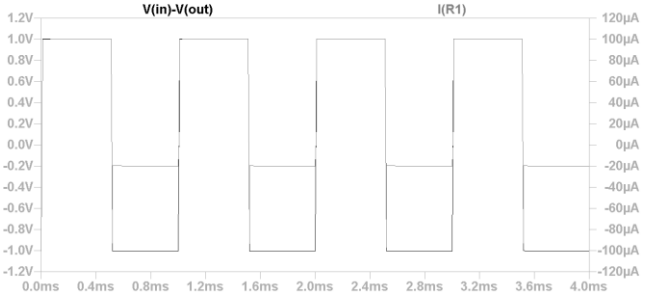

Fig. 8. Voltage across memristor and current through it for pulse wave voltage excitation

Observing the obtained output current waveforms leads to several conclusions. First, glitches are seen at the points of switching from low resistance to high resistance and not from low to high resistance, for both excitations, but more frequently and with higher amplitude in the case of pulse wave. In the case of square pulse input, one can notice that the memristor starts functioning earlier, i. e. switches its resistive state at the first change of voltage level (from higher to lower), but this is only because at the beginning of the transient analysis, the voltage rises from 0V (initial condition) to the set high level of 1.005V, so there is actually another change of voltage that should but does not induce a change of resistance.

IV. Conclusion

In this paper a new and simplified Spice model of memristor is introduced. It relies on functionality of an ideal memristor as a two-state (resistance) switch. It is parameterised by both on and off resistances and the switching voltage threshold, which is immensely useful for behavioural analysis in the initial phases of the circuit design. Also, the model accurately expresses the basic characteristics of a memristor component, and can be used for educational purposes. A disadvantage of the model is identified as a possibility to induce a significantly slow transient analysis in a more complex design, because of the flip-flop based circuitry.

Further research regarding this topic would be the simulation and the verification of some circuits incorporating this memristor model. A good start would be a simple analogue circuit, such as MC (memristor-capacitor) filters, or more complex circuits such as programmable analogue amplifier. Further, the model could be made more sophisticated if flip-flops which slow down the transient analysis are to be replaced with a faster alternative.

Appendix

The netlist of the Spice model of memristor described in this paper is as follows:

```
.SUBCKT memristor_simple pin1 pin2
+PARAMS: Vlim=0.4 ton=1m Ron=10
+Roff=50
Gout pin1 pin2 out 0 1
B1 compH 0 V={if(V(pin1)-
+V(pin2)>{Vlim},1,0)}
B2 compL 0 V={if(V(pin1)-V(pin2)<-
+{Vlim},1,0)}
A1 N001 0 clk 0 0 0 prev 0 DFLOP
V2 clk 0 PULSE(0 1 0 {ton/2} {ton/2}
+{ton} {ton*2-2*ton/10})
B3 compHN 0 V={if(V(pin1)-
+V(pin2)<{Vlim},1,0)}
B4 compLN 0 V={if(V(pin1)-V(pin2)>-
+{Vlim},1,0)}
A2 compHN compLN 0 0 0 0 N001 0 AND
B6 stay 0 V={if((V(prev)==1 &
+V(compH)==0 & V(compL)==0) |
+(V(prev)==0), 1, 0)}
B8 onoff 0 V={if(abs((V(pin1)-
+V(pin2))/V(out)-{Ron}) <
+abs((V(pin1)-V(pin2))/V(out)-{Roff})
+, 0, 1)}
B10 res 0 V={V(onoff)*({Roff}-{Ron})
++ {Ron}}
B12 currS 0 V={if(V(stay)==1,
+(V(pin1)-V(pin2))/V(res),0)}
B13 currH 0 V={if(V(compH)==1 &
+V(stay)==0,{Vlim}/{Ron},0)}
B14 currL 0 V={if(V(compL)==1 &
+V(stay)==0,-{Vlim}/{Roff},0)}
B5 out 0 V={V(currS)+V(currH)+
+V(currL)}
.ENDS memristor_simple
```

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